

**In the Claims:**

No amendments to the claims are presented.

1. (Previously Presented) A resistor network comprising:
  - a resistor body that includes multiple resistor sub-bodies, and
  - a plurality of columns of taps,
  - each of the resistor sub-bodies situated between two of the columns of taps and connected to each of the taps of the two columns of taps, with electrical connection between respective sub-bodies being exclusively via the taps connected to the respective resistor sub-bodies,
  - wherein at least two of the taps are configured to be connected with respective first and second sources of reference input potentials, and
  - wherein each tap of the columns of taps is configured for outputting an output potential via a contact area which is connected with the concerning tap.
2. (Previously presented) A resistor network according to claim 1, wherein each tap of the columns of taps is a T-shaped or S-shaped projection which is connected with one of the resistor sub-bodies.
3. (Previously Presented) A resistor network according to claim 1, characterised in that, a plurality of taps of a first column of taps of a first resistor sub-body is connected with a plurality of taps of a second column of taps of a second resistor sub-body, wherein each tap of the plurality of taps of the first column is connected with only one tap of the plurality of taps of the second column and wherein each tap of the plurality of taps of the second column is connected with only one tap of the plurality of taps of the first column.
4. (Previously Presented) A resistor network according to claim 3, characterised in that, each tap of the first column is shifted at least one column position with respect to the column position of the tap of the second column with which the tap of the first column is connected.

5. (Previously Presented) A resistor network according to claim 3, characterised in that, the respective connections between the resistor sub-bodies with the taps are made during fabrication of the resistor network at different arbitrary positions with respect to the respective taps.

6. (Previously Presented) A resistor network according to claim 1, characterised in that, the resistor network is a semiconductor circuit, wherein each resistor sub-body comprises a number of resistor layers, wherein each semi-conducting resistor layer comprises at least two taps, and wherein the semi-conducting resistor layers are interconnected via the taps.

7. (Previously Presented) An Analog-Digital converter for generating a digital output signal on the basis of an analog input signal, characterised in that, the Analog-Digital converter comprises a resistor network having

- a resistor body that includes multiple resistor sub-bodies, and
- a plurality of columns of taps, each of the resistor sub-bodies situated between two of the columns of taps and connected to each of the taps of the two columns of taps, wherein at least two of the taps are configured to be connected with respective first and second sources of reference input potentials,

- wherein each tap of the columns of taps is configured for outputting an output potential via a contact area which is connected with the concerning tap, and

- wherein electrical connection between the resistor sub-bodies are exclusively via the taps connected with the resistor sub-bodies.

8. (Previously Presented) A Digital-Analog converter for generating an analog output signal on the basis of a digital input signal, characterised in that, the Digital-Analog converter comprises a resistor network having

- a resistor body that includes multiple resistor sub-bodies, and
- a plurality of columns of taps, each of the resistor sub-bodies situated between two of the columns of taps and connected to each of the taps of the two columns of taps,

wherein at least two of the taps are configured to be connected with respective first and second sources of reference input potentials,

wherein each tap of the columns of taps is configured for outputting an output potential via a contact area which is connected with the concerning tap, and

wherein electrical connection between the resistor sub-bodies are exclusively via the taps connected with the resistor sub-bodies.

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Previously presented) A resistor ladder network, comprising:

a resistor body that includes multiple resistor sub-bodies; and

a plurality of columns of taps, each of the resistor sub-bodies situated between two of the columns of taps and connected to each of the taps of the two columns of taps, the columns of taps arranged in parallel to and alternating with the resistor sub-bodies,

wherein at least two of the taps are configured to be connected with respective first and second sources of reference input potentials, each tap of the columns of taps is configured for outputting an output potential via a contact area which is connected with the concerning tap, and the only electrical connections between the resistor sub-bodies are electrical connections via the taps connected to the resistor sub-bodies.

13. (Previously presented) A resistor ladder network according to claim 12, wherein each tap of the columns of taps is a T-shaped or S-shaped projection which is connected with one of the resistor sub-bodies and each of the columns of taps includes at least three taps.

14. (Previously presented) A resistor ladder network according to claim 12, wherein a plurality of taps of a first one of the columns of taps connected to a first one of the resistor sub-bodies is connected with a plurality of taps of a second one of the columns of

taps connected a second one of the resistor sub-bodies, each tap of the first column connected with only one of the taps of the second column.

15. (Previously presented) A resistor ladder network according to claim 14, wherein each tap of the first column is shifted at least one column position with respect to a column position of the tap of the second column with which the tap of the first column is connected.

16. (Previously Presented) A resistor network according to claim 1, wherein each of the taps is connected to at most two resistor sub-bodies, and wherein each resistor sub-body is connected to a plurality of taps.